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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,451	12/05/2003	Roy E. Scheuerlein	MA-112	9337

7590 03/27/2006

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Santa Clara, CA 95054

EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,451	SCHEUERLEIN ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-29,33-43,46-55,59-73,75-80 and 83-93* is/are pending in the application.

4a) Of the above claim(s) *16-26,46-54,70-72 and 75-80* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-15,27-29,33-43,55,59-69,73,83-93* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I and Species IA in the reply filed on 7/15/05 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 6, 33, 34, 59, 60, 83 and 84 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwasaki (US Patent No. 6,034,436).

With regard to claim 6, Iwasaki disclose in figure 7B a structure for providing multilevel electrical connectivity within an integrated circuit (note that figure 7B shows a portion of a cross section that will repeat many times on the chip), the structure comprising:

- a first plurality of vias D1/D3, each having a top end and a bottom end;
- a second plurality of vias D2, each having a top end and a bottom end, wherein the first and second pluralities of vias are vertically overlapping;
- a first routing level S2 at a first height, the first level connected to the first plurality of vias at the bottom end of each first via;

- a second routing level S1 at a second height connected to the second plurality of vias at the bottom end of each second via, wherein the first height is different from the second height;
- where both routing levels are formed above the substrate
- wherein the first and second vias are evenly spaced and have a common first pitch;
- and further comprising a third routing level U1/U2/U3, the third routing level above the first and second vias connected at the top end of each first and second via, vertically opposite the first and second routing levels;
- wherein the third routing level comprises memory lines in a memory array.

Iwasaki discloses an improved through hole structure and teaches that through hole/interconnect structures are used for memory arrays. Thus, the third routing levels are considered "memory lines" as they are conductive lines used in a memory array.

With regard to claim 33, this claim is rejected similar to claim 6 above. Note that the first, second and third routing levels are formed above the substrate.

With regard to claim 34, the first routing level has a second pitch and the second routing level has a third pitch, the first pitch smaller than the second and third pitch.

With regard to claims 59 and 60, these claims are anticipated in a manner similar to claim 6 above.

With regard to claims 83 and 84, Iwasaki disclose a method for forming the device as claimed including forming the first and second routing levels with the second routing level above the first, and forming first and second pluralities of vias connected at

bottom ends to the routing levels, wherein the first and second pluralities of vias are vertically overlapping. These claims are rejected similarly to claim 6 above.

4. Claims 6, 7, 15, 28, 29, 33-35, 43, 59, 69, 83-85 and 86 are rejected under 35 U.S.C. 102(b) as being anticipated by Amanuma (US 2001/0038115 A1).

Amanuma discloses a device as claimed in figure 2, for example. The cross section in figure 2 shows a portion of the repeating structure of an array, thus this cross section is repeated many times. With regard to claim 6, Amanuma discloses:

- a first plurality of vias each having a top end and a bottom end (12 on the right side of the transistors formed below; the first vias are considered to extend from the bottom of structure 30 to the top of structure 10);
- a second plurality of vias each having a top end and a bottom end (12 on the left side of the transistors formed below; the second vias are considered to extend from the bottom of structure 30 to the top of structure 7), wherein the first plurality of vias and the second plurality of vias are vertically overlapping;
- a first routing level at a first height (10) connected to the first plurality of vias at the bottom end of each first via;
- a second routing level at a second height (7) connected to the second plurality of vias at the bottom end of each second via, where the first height is different from the second height;
- wherein both routing levels are formed above the substrate;

- wherein the first and second vias are evenly spaced and have a common first pitch;
- and further comprising a third routing level 18, the third routing level above the first and second vias connected at the top end of each first and second via vertically opposite the first and second routing levels;
- wherein the third routing level comprises memory lines in a memory array.

With regard to claims 7, wherein memory cells accessed by the memory lines are charge storage memory cells (capacitors).

With regard to claims 15, 28 and 29, the memory lines have a fourth pitch smaller than the first pitch, further wherein the fourth pitch is substantially one half the first pitch.

With regard to claims 33 and 34, this claim is rejected similarly to claim 6 above.

With regard to claim 35, the third routing level comprises memory lines in a memory array where cells accessed by the memory lines are charge storage cells (capacitors).

With regard to claim 43, the memory lines have a fourth pitch smaller than the first pitch.

With regard to claim 59, this claim is anticipated in a manner similar to claim 6 above.

With regard to claim 69, the memory lines have a fourth pitch smaller than the first pitch.

With regard to claims 83 and 84, Amanuma discloses a method for forming the device as claimed including forming the first and second routing levels with the second

routing level above the first, and forming first and second pluralities of vias connected at bottom ends to the routing levels, wherein the first and second pluralities of vias are vertically overlapping. This claim is rejected similarly to claim 6 above.

With regard to claim 85, the memory lines have a third pitch smaller than the first pitch.

With regard to claim 86, the third routing level comprises memory lines in a memory array where cells accessed by the memory lines are charge storage cells (capacitors).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7-14, 27, 35-42, 55, 61-68, 73 and 86-93 rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki as applied to claims 6, 33, 34, 59, 60, 83 and 84 above.

Iwasaki teach the structure of the interconnections with first, second and third routing levels and first and second pluralities of vias. However, Iwasaki does not teach the particular device that the interconnects are used to connect. Thus, Iwasaki does not explicitly teach the memory cells being charge storage memory cells, SONOS devices, floating gate devices, arranged in a NAND string, passive element memory cells

including a fuse or antifuse, of a monolithic three dimensional memory array which further comprises at least first and second memory levels with the second memory level formed above the first. Though not explicitly taught by the reference, it is considered nonetheless obvious to one of ordinary skill in the art to employ the improved through-hole structure of Iwasaki to any known memory device structure and array. There is nothing inventive in using a known through-hole structure for semiconductor devices in any of the claimed variety of memory cells and arrays. One of ordinary skill in the art would have found it obvious to combine the through-hole layout of Iwasaki into the known memory arrays and structures in order to reduce the occupied area for the interconnections.

Response to Arguments

7. Applicant's arguments filed 1/5/06been fully considered but they are not persuasive.

Applicant has argued that the third routing levels U1/U2/U3 or Iwasaki are not memory lines. This argument is not persuasive. The claims do not recite any particular structure for the "memory lines" except that they are routing levels. Thus, the conductive routing levels U1/U2/U3 of Iwasaki are considered "memory lines". Further, as stated by applicant in their arguments, "such memory lines may be conductors;" see page 24 line 14 of applicant's response. Since the routing levels U1/U2/U3 of Iwasaki are conductors they read on the claimed "memory lines." Still further, the term "memory lines" is an intended use of the claimed routing levels. The claims do not require that

the lines themselves provide any memory storage. Thus, a conductive line used in a memory can be properly considered "memory lines." The lines of Iwasaki are conductive lines used as interconnections in a memory array and thus are considered memory lines.

Applicant has also argued that Amanuma does not teach the claimed structure since applicant interprets the vias of Amanuma to have bottom ends at the same level, and thus the first and second routing levels at the same height instead of the claimed different heights. This is not persuasive. As explained in the rejection above, the first via is via 12 on the right side of the transistors formed below, the first vias are considered to extend from the bottom of structure 30 to the top of structure 10. Thus the routing level is routing level 10. The second via 12 is considered the via on the left side of the transistors extending from the bottom of structure 30 to the top of structure 7 and the second routing level is considered routing level 7. Thus, the vias are vertically overlapping and have bottom ends (at which the first and second routing levels are formed) that are at different heights. It is noted that applicant is interpreting Amanuma in a narrow manner so as to reason that it does not read on the claims. The rejection relies upon a proper, reasonably broad interpretation that shows how the claims as written as so broad so as to read on Amanuma.

Applicant has also argued that the rejection under 35 U.S.C. 103(a) of claim 14 is improper. Applicant argues that the fact that an interconnect structure such as that of

Iwasaki is known does not make it obvious to use in every memory array, specifically the monolithic three dimensional memory array of claim 14. Applicant argues that the complexity of interconnect fabrication and layout constraints will lead one skilled in the art to choose other interconnect methods. Applicant points to four references as teaching the three dimensional memory array that do not use the interconnect structure of Iwasaki and states that absent some motivation (suggestion) that the interconnects of Iwasaki are advantageous in this context (with the three dimensional memory array), a *prima facie* case of obviousness has not been made. The examiner agrees that if no motivation or advantage has been provided for using the interconnect structure of Iwasaki in the three dimensional memory array, a *prima facie* case of obviousness would not have been made. However, in this case motivation for using the particular interconnect structure claimed (that of Iwasaki) has been provided in the rejection, and thus a *prima facie* case of obviousness has indeed been established. As stated in the rejection, one would desire using the interconnect structure of Iwasaki in order to reduce the occupied area for the interconnections (see Iwasaki abstract, last sentence, for example). As one of ordinary skill would recognize, this is advantageous as it allows the memory array to be formed in a smaller area and thus allows for higher device packing and density.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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